AMENDMENT TO THE CLAIMS

Claims 1 - 12. (Cancelled)

13. (Currently Amended) ~~The semiconductor device according to claim 12~~ A semiconductor device comprising:

a pair of source/drain regions formed on the main surface of a silicon region at a prescribed interval to define a channel region and lifted up in an elevated structure;

a gate insulator film, formed on said channel region, consisting of a high dielectric constant insulator film having a dielectric constant larger than 3.9;

a gate electrode including a first metal layer coming into contact with said gate insulator film and having a work function controlled to have a Fermi level around the energy level of a band gap end of silicon constituting said source/drain regions; and

source/drain electrodes, formed on the upper surfaces of said pair of source/drain regions having the elevated structure to be in contact with the upper surfaces of said pair of source/drain regions without interposition of metal silicide films, including third metal layers having a work function controlled to have a Fermi level around the energy level of the band gap end of silicon constituting said source/drain regions, wherein

said source/drain regions include n-type source/drain regions;

said source/drain electrodes include said third metal layers having said work function controlled to have a Fermi level around the energy level of the conduction band of silicon; and

said third metal layers include Hf layers.

14. (Currently Amended) ~~The semiconductor device according to claim 11~~ A semiconductor device comprising:

a pair of source/drain regions formed on the main surface of a silicon region at a prescribed interval to define a channel region and lifted up in an elevated structure;

a gate insulator film, formed on said channel region, consisting of a high dielectric constant insulator film having a dielectric constant larger than 3.9;

a gate electrode including a first metal layer coming into contact with said gate insulator film and having a work function controlled to have a Fermi level around the energy level of a band gap end of silicon constituting said source/drain regions; and

source/drain electrodes, formed on the upper surfaces of said pair of source/drain regions having the elevated structure to be in contact with the upper surfaces of said pair of source/drain regions without interposition of metal silicide films, including third metal layers having a work function controlled to have a Fermi level around the energy level of the band gap end of silicon constituting said source/drain regions, wherein

said source/drain regions include p-type source/drain regions, and

said source/drain electrodes include said third metal layers having said work function controlled to have a Fermi level around the energy level of the valence band of silicon.

15. (Original) The semiconductor device according to claim 14, wherein

said third metal layers include either Ni layers or Ir layers.

16. (Currently Amended) ~~The semiconductor device according to claim 11~~ A semiconductor device comprising:

a pair of source/drain regions formed on the main surface of a silicon region at a prescribed interval to define a channel region and lifted up in an elevated structure;

a gate insulator film, formed on said channel region, consisting of a high dielectric constant insulator film having a dielectric constant larger than 3.9;

a gate electrode including a first metal layer coming into contact with said gate insulator film and having a work function controlled to have a Fermi level around the energy level of a band gap end of silicon constituting said source/drain regions; and

source/drain electrodes, formed on the upper surfaces of said pair of source/drain regions having the elevated structure to be in contact with the upper surfaces of said pair of source/drain regions without interposition of metal silicide films, including third metal layers having a work function controlled to have a Fermi level around the energy level of the band gap end of silicon constituting said source/drain regions, wherein

said pair of source/drain regions having the elevated structure include:

said third metal layers having said controlled work function, and

fourth metal layers, formed on said third metal layers, having a larger thickness than said third metal layers.

17. (Original) The semiconductor device according to claim 16, wherein

said fourth metal layers are metal layers having an uncontrolled work function.

18. (Original) The semiconductor device according to claim 16, wherein

said fourth metal layers include at least either TaN layers or TiN layers.

Claims 19- 25. (Cancelled)